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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

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Assistant Commissioner for Patents

Washington, D.C. 20231

Serial No.: 09/847,622

Filed: May 2, 2001

For: FIELD EFFECT TRANSISTOR WITH

REDUCED GATE DELAY AND METHOD OF FABRICATING THE

SAME

Examiner: Walter Lee Lindsay, Jr.

Group Art Unit: 2812

Att'y Docket: 2000.064200/DE06\$3

RESPONSE TO RESTRICTION
REQUIREMENT DATED FEBRUARY 26, 2002

CERTIFICATE OF MAILING

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as "FIRST CLASS MAIL" addressed to: Assistant Commissioner for Patents, Washington, DC 20231, this 7th day of March, 2002.

Sir:

Signature

This paper is submitted in response to the Restriction Requirement dated February 26, 2002, for which the one-month date for response is March 26, 2002.

In response to the restriction requirement which the Examiner imposed, Applicants elect, with traverse, to prosecute claims 1-9 and 27-34, *i.e.*, the Group I claims.

It is believed that no fee is due; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to this document, the Assistant Commissioner is authorized to deduct said fees from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/DE0053. In the event the monies in that account are insufficient, the Assistant Commissioner is authorized to

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withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.064200.

The Examiner is invited to contact the undersigned attorney at (713) 934-4055 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: March 7, 2002

J. Mike Amerson Reg. No. 35,426

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